IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below for the Examiner's convenience. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please **AMEND** claim 1 in accordance with the following:

Claim 1 (Currently Amended): An apparatus detecting binary data from an input signal read from an optical recording medium, the apparatus comprising:

a first signal processor arranged to nonlinearly convert the input signal based on a result of comparing an absolute value of the input signal and a predetermined critical value, and generate a nonlinearly converted signal; and

a second signal processor arranged to detect binary data from the nonlinearly converted signal representing information stored on the optical recording medium,

wherein a difference between the absolute value of the ~~digital~~input signal and the predetermined critical value is output as the nonlinearly converted signal when the absolute value of the ~~digital~~input signal is larger than the predetermined critical value and the ~~digital~~ input signal is greater than zero (0),

wherein a summation of the absolute value of the ~~digital~~input signal and the predetermined critical value is output as the nonlinearly converted signal when the absolute value of the ~~digital~~input signal is larger than the predetermined critical value and the ~~digital~~input signal is less than zero (0), and

wherein zero(0) is output as the nonlinearly converted signal when the absolute value of the ~~digital~~input signal is not greater than the predetermined critical value.

Claim 2 (Previously Presented): The apparatus of claim 1, wherein the first signal processor saturates the input signal by the predetermined critical value when the absolute value of the input signal is larger than the predetermined critical value, and outputs the input signal as the nonlinearly converted signal when the absolute value of the input signal is smaller than the predetermined critical value.

Claim 3 (Canceled):

Claim 4 (Previously Presented): The apparatus of claim 2, wherein the first signal processor includes a digital filter using a nonlinear function that yields the result of the following equation:

$$y = x \times \{|x| \leq k\} + k(-1)^{(|x| \leq 0)} \times \{|x| > k\}$$

wherein | | indicates an absolute value, the braces and contents become one (1) if a conditional expression contained therein is true, and zero (0) if a conditional expression contained therein is false, *x* is the input signal, and k is the predetermined critical value ranging from zero (0) to a positive real number.

Claim 5 (Previously Presented): The apparatus of claim 1, wherein the first signal processor includes a digital filter using a nonlinear function that yields the result of the following equation:

$$y = x \times \{|x| > k\} + k(-1)^{(|x| > 0)} \times \{|x| > k\}$$

wherein | | indicates an absolute value, the braces and contents become one (1) if a conditional expression contained therein is true, and zero (0) if a conditional expression contained therein is false, *x* is the input signal, k and is the predetermined critical value ranging from zero to a positive real number.

Claim 6 (Previously Presented): The apparatus of claim 1, wherein the first signal processor is a digital filter using a nonlinear function.

Claim 7 (Previously Presented): The apparatus of claim 1, wherein the first signal processor comprises:

at least one finite impulse response (FIR) filter arranged to change frequency characteristics of the input signal; and

a nonlinear filter arranged to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value.

Claim 8 (Previously Presented): The apparatus of claim 2, wherein the first signal processor comprises:

first and second finite impulse response (FIR) filters arranged in series to change frequency characteristics of the input signal; and

a nonlinear filter disposed between the first and second FIR filters, to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value.

Claim 9 (Previously Presented): The apparatus of claim 6, wherein the first signal processor further comprises a finite impulse response (FIR) filter arranged in front of the digital filter to change frequency characteristics of the input signal.

Claim 10 (Previously Presented): The apparatus of claim 6, wherein the first signal processor further comprises a finite impulse response (FIR) filter arranged behind the digital filter to change frequency characteristics of the input signal.

Claim 11 (Previously Presented): The apparatus of claim 2, wherein the first signal processor comprises:

a nonlinear filter to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value; and

finite impulse response (FIR) filters arranged in front, behind and in parallel with the nonlinear filter respectively, to change frequency characteristics of the input signal.

Claim 12 (Previously Presented): The apparatus of claim 1, wherein the first signal processor comprises:

a nonlinear filter to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value; and

finite impulse response (FIR) filters arranged behind and in parallel with the nonlinear filter respectively, to change frequency characteristics of the input signal.

Claim 13 (Previously Presented): The apparatus of claim 1, wherein the first signal

processor comprises:

a nonlinear filter to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value;

first and second finite impulse response (FIR) filters arranged in series behind with the nonlinear filter; and

a third FIR filter arranged in parallel with the nonlinear filter,

wherein the first, second and third FIR filters are configured to change frequency characteristics of the input signal.

Claim 14 (Previously Presented): The apparatus of claim 2, further comprising an equalizer disposed between the first signal processor and the second signal processor to condition the nonlinearly converted signal and to output a partial response sampled signal to the second signal processor for data detection.

Claim 15 (Previously Presented): The apparatus of claim 1, further comprising an equalizer disposed between the first signal processor and the second signal processor to condition the nonlinearly converted signal and to output a partial response sampled signal to the second signal processor for data detection.

Claim 16 (Previously Presented): The apparatus of claim 1, wherein the second signal processor is a Viberti decoder employing one of a PR (a,b,a) method, a PR (a,b,b,a,) method, and a PR (a,b,c,b,a) method.

Claim 17 (Previously Presented): The apparatus of claim 16, wherein the Viterbi decoder further uses an equalizer to adjust the frequency characteristics of the input signal.

Claims 18-19 (Canceled):

Claim 20 (Previously Presented): A method of detecting binary data from an input signal read from an optical recording medium, the method comprising:

converting an input signal read from the optical recording medium into a digital signal;

converting the digital signal nonlinearly based on a result of comparing an absolute value

of the digital signal and a predetermined critical value into a nonlinearly converted signal, using a nonlinear filter; and

detecting binary data from the nonlinearly converted signal representing information stored on the optical recording medium,

wherein a difference between the absolute value of the digital signal and the predetermined critical value is output as the nonlinearly converted signal when the absolute value of the digital signal is larger than the predetermined critical value and the digital signal is greater than zero (0), a summation of the absolute value of the digital signal and the predetermined critical value is output as the nonlinearly converted signal when the absolute value of the digital signal is larger than the predetermined critical value and the digital signal is less than zero (0), and zero (0) is output as the nonlinearly converted signal when the absolute value of the digital signal is not greater than the predetermined critical value.

Claim 21 (Previously Presented): The method of detecting binary data of claim 20, wherein the conversion of the digital signal is executed, via a digital filter having a nonlinear function, according to the following equation:

$$y = x \times \{|x| \leq k\} + k(-1)^{(|x| \leq 0)} \times \{|x| > k\}$$

wherein | | indicates an absolute value, the braces and contents become one (1) if a conditional expression contained therein is true, and zero (0) if a conditional expression contained therein is false, x is the digital signal, and k is the predetermined critical value ranging from zero (0) to a positive real number.

Claim 22 (Previously Presented): The method of detecting binary data of claim 20, wherein the conversion of the digital signal is executed, via a digital filter having a nonlinear function, according to the following equation:

$$y = x \times \{|x| > k\} + k(-1)^{(|x| > 0)} \times \{|x| > k\}$$

wherein | | indicates the absolute value, the braces and contents become one (1) if the conditional expression contained therein is true, and zero (0) if the conditional expression contained therein is false, x is the digital signal, and k is the predetermined critical value ranging from zero (0) to a positive real number.

Claims 23-25 (Canceled):